What is claimed is:

1. A memory device comprising:

a memory array comprised of an array of memory cells, wherein the memory array generates leakage current during a suspend mode of operation;

a sinking suspend voltage regulator that generates a sinking suspend voltage;

a gate-sinking voltage keeper component that controllably connects the memory array to the sinking suspend voltage regulator during the suspend state and that operates as a leakage current sink; and

a controller component connected to the gate-sinking voltage keeper component to controllably bias the gate-sinking voltage keeper component, thereby activating the gate-sinking voltage keeper component which in response couples the sinking suspend voltage to a portion of the memory array upon initiation of the suspend mode.

2. The memory device of claim 1, wherein the gate-sinking voltage keeper component comprises a pmos transistor.

3. The memory device of claim 2, wherein a gate of the pmos transistor is connected to a control signal generated by the controller component.

4. The memory device of claim 3, wherein the control signal is asserted during the suspend mode of operation.

5. The memory device of claim 1, wherein the gate-sinking voltage keeper component electrically connects to an array supply voltage input of the memory array.

6. The memory device of claim 1, wherein the gate-sinking voltage keeper component electrically connects to a word line of the memory array.

7. The memory device of claim 1, further comprising one or more additional gate-sinking voltage keeper components that controllably connect bit lines of the memory array to the suspend voltage regulator.

8. The memory device of claim 1, wherein the suspend voltage is about 0.3 to 0.8 volts.

9. The memory device of claim 1, wherein a VDDA input of the memory array is biased to a normal mode voltage during a normal mode and to a sourcing suspend voltage during the suspend mode of operation.

10. The memory device of claim 9, wherein the normal mode voltage is about 1.3 to 1.0 volts and the sourcing suspend voltage is about 0.7 to 0.4 volts below the normal mode voltage.

11. The memory device of claim 1, further comprising a footer switch that controllably connects a VSS voltage to a VSSA input of the memory array.

12. The memory device of claim 1, further comprising row periphery circuitry that addresses one or more of the memory cells during normal mode.

13. The memory device of claim 1, wherein the sinking suspend voltage regulator is further operable as a leakage current sink to dissipate leakage current not sunk by the gate-sinking voltage keeper component.

14. The memory device of claim 13, wherein the sinking suspend voltage regulator is a low-dropout voltage regulator.

15. The memory device of claim 1, further comprising a gate-sourcing voltage keeper and a sourcing suspend voltage regulator that generates a sourcing suspend voltage, wherein the gate-sourcing voltage keeper connects the sourcing voltage to a VDDA input of the memory array during the suspend mode.

16. A method of operating a memory device in a suspend mode of operation comprising:

biasing one or more inputs of a memory array to a sinking suspend voltage by one or more gate-sinking voltage keeper components;

generating leakage current by the memory array; and

sinking at least a portion of generated leakage current from the memory array by the one or more gate-sinking voltage keeper components.

17. The method of claim 16, wherein biasing one or more inputs comprises selectively coupling the sinking suspend voltage to the one or more inputs of the memory array by the one or more gate-sinking voltage keeper components.

18. The method of claim 16, further comprising:

connecting a VSSA input of the memory array to the sinking suspend voltage *via* one of the gate-sinking voltage keeper components.

19. The method of claim 16, further comprising generating a suspend mode of operation control signal that selectively controls the one or more gate-sinking voltage keeper components.

20. The method of claim 16, further comprising generating the sinking suspend voltage by a low-dropout voltage regulator.

21. The method of claim 16, further comprising sinking a remaining portion of the generated leakage current.

22. The method of claim 16, further comprising isolating a VSSA input from a normal mode array voltage supply.

23. A method of operating a memory device comprising:

biasing a VSSA input of a memory array to a normal array mode voltage during normal mode;

isolating the VSSA input and a word line from a sinking suspend voltage by one or more gate-sinking voltage keeper components during the normal mode;

initiating a suspend mode of operation;

isolating the VSSA input of the memory array from the normal array mode voltage during the suspend mode of operation;

biasing the VSSA input to the sinking suspend voltage during the suspend mode of operation;

biasing the word line to the sinking suspend voltage during the suspend mode of operation.

generating leakage current by the memory array during the suspend mode of operation; and

sinking at least a portion of the generated leakage current by one or more gate-sinking voltage keeper components.

24. The method of claim 23, further comprising:

biasing a VDDA input to a normal mode supply voltage during the normal mode; and

biasing the VDDA input to a sourcing suspend voltage via a gate-sourcing voltage keeper during the suspend mode of operation.

25. The method of claim 23, wherein the VSSA input is biased to the sinking suspend voltage by one of the gate-sinking voltage keeper components.